

TECHNICAL DOCUMENT 3196
April 2005

**DC and RF Characterization
of Laser Annealed
Metal-Gate SOI CMOS
Field-Effect Transistors**

R. P. Lu
B. W. Offord
J. D. Popp
A. D. Ramirez
J. F. Rowland
S. D. Russell

Approved for public release;
distribution is unlimited.

SSC San Diego

TECHNICAL DOCUMENT 3196
April 2005

**DC and RF Characterization
of Laser Annealed
Metal-Gate SOI CMOS
Field-Effect Transistors**

R. P. Lu
B. W. Offord
J. D. Popp
A. D. Ramirez
J. F. Rowland
S. D. Russell

Approved for public release;
distribution is unlimited.



SSC San Diego
San Diego, CA 92152-5001

SSC SAN DIEGO
San Diego, California 92152-5001

T. V. Flynn, CAPT, USN
Commanding Officer

R. F. Smith
Executive Director

ADMINISTRATIVE INFORMATION

The work described in this report was performed for the Office of Naval Research Internal Applied Research (IAR) Program by the Electromagnetics & Advanced Technology Division (Code 2853) of SPAWAR Systems Center San Diego (SSC San Diego).

Released under authority of
S. D. Russell, Head
Electromagnetics & Advanced
Technology Division

This is a work of the United States Government and therefore is not copyrighted. This work may be copied and disseminated without restriction. Many SSC San Diego public release documents are available in electronic format at <http://www.spawar.navy.mil/sti/publications/pubs/index.html>

DC and RF Characterization of Laser Annealed Metal-Gate SOI CMOS Field-Effect Transistors

*Ryan P. Lu, Bruce W. Offord, Jeremy Popp, Ayax D. Ramirez,
Jason Rowland, Stephen D. Russell*

Space and Naval Warfare Systems Center
San Diego

American Physical Society
21–25 March 2005, Los Angeles, CA

Abstract

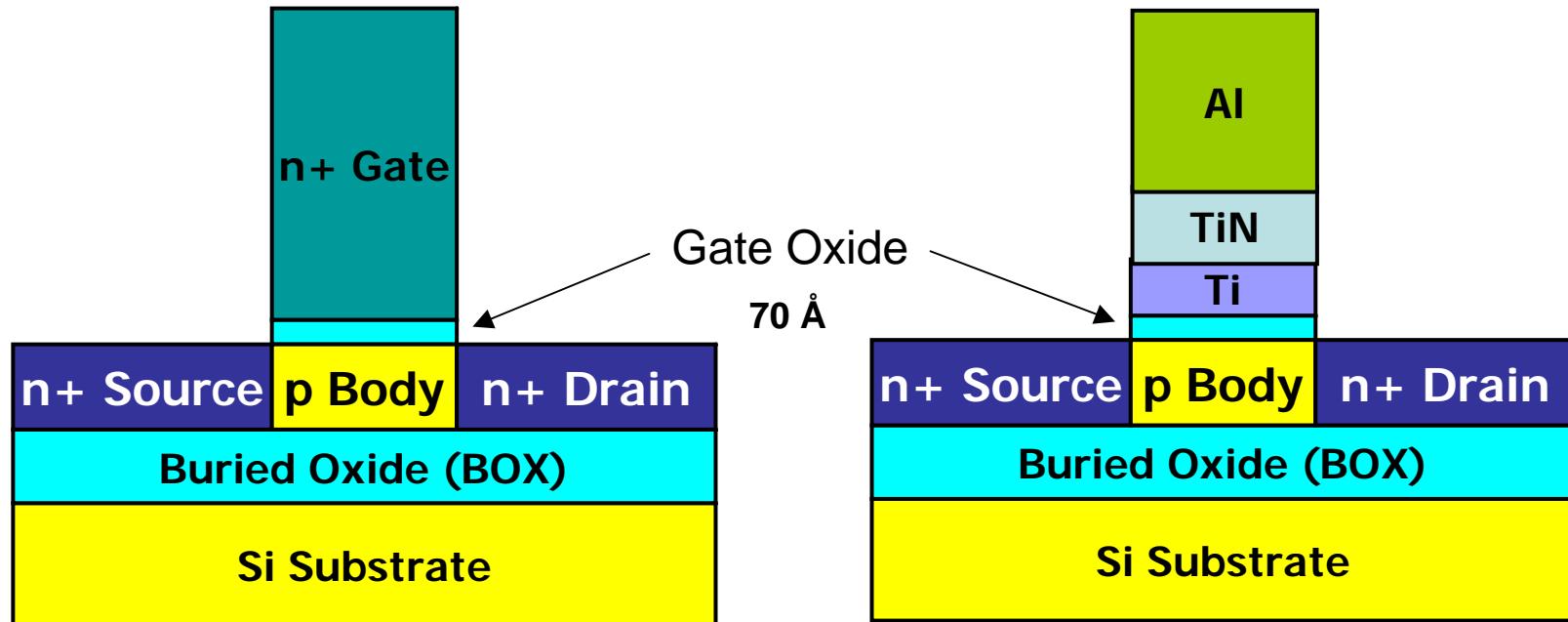
The conventional polysilicon gate in a MOSFET has been replaced by an aluminum metal gate which offers higher RF performance through the reduction of gate resistance. Pulsed excimer laser annealing of the source and drain was then used to avoid conventional furnace annealing that would melt the aluminum metal gate. CMOS field-effect transistors utilizing metal gates were fabricated in Silicon-on-Insulator (SOI) technology down to 0.25-micron gate lengths. The DC characteristics of devices with 10-micron gate lengths were consistently well-behaved. The 0.25-micron devices were found to be more sensitive to the laser energy that showed up in the DC measurements in threshold voltage variations and larger leakage currents in the subthreshold characteristics. At higher laser fluences, Technology Computer-Aided Design (TCAD) simulations show excessive lateral diffusion, explaining the observed effects. RF results of the drawn 0.25-micron metal-gate devices have an F_t and F_{max} of 25 GHz and 60 GHz, respectively. Similar devices with polysilicon gates were fabricated and characterized for comparison. RF results of the drawn 0.25-micron polysilicon-gate devices have an F_t and F_{max} of 34 GHz and 7 GHz, respectively. This device processing advance offers a deeply scalable technology for future “system-on-a-chip” applications.

Why use SOI?

As devices are scaled down in size, MOSFET performance suffers from short channel effects and the parasitic resistances and capacitances become more apparent in RF applications. These parasitics limits the potential to achieve a high cutoff frequency and power gain, F_t and F_{max} , respectively. Silicon-on-insulator technology reduces the short channel effects as well as parasitic junction capacitances for improved microwave frequency figures of merit.

Why use Metal Gates?

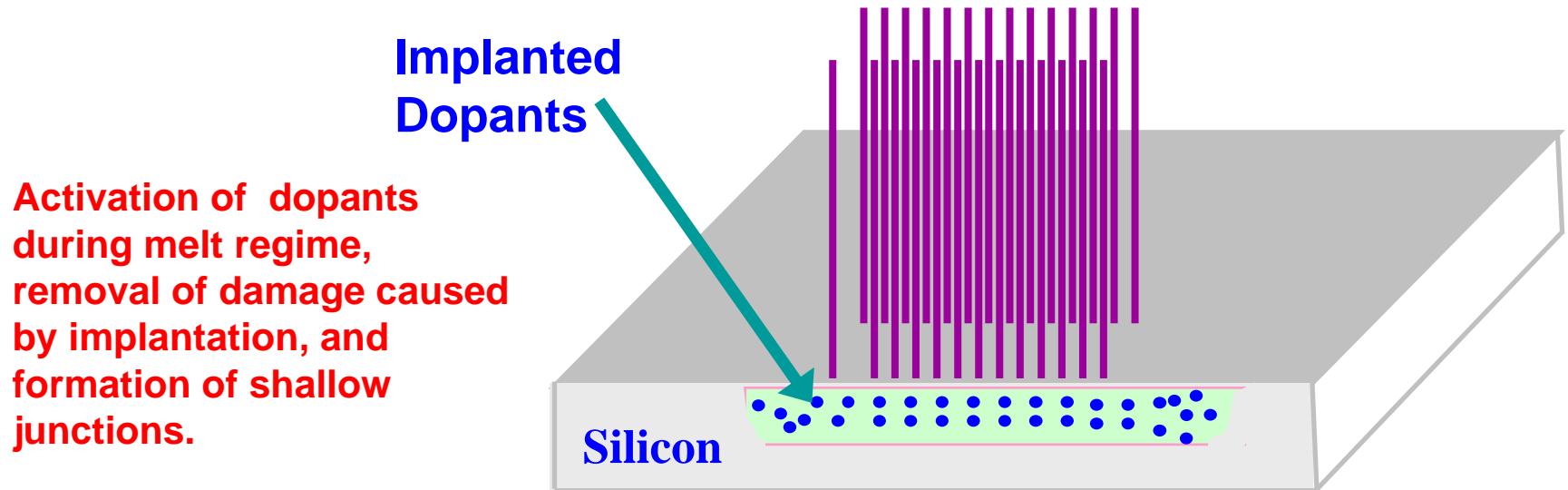
Using Al as the material for the metal gate creates a device that has at least an order of magnitude lower gate resistance than a silicide polygate. Reducing the gate resistance directly improves the RF performance of the device.



Why Use Laser Annealing?

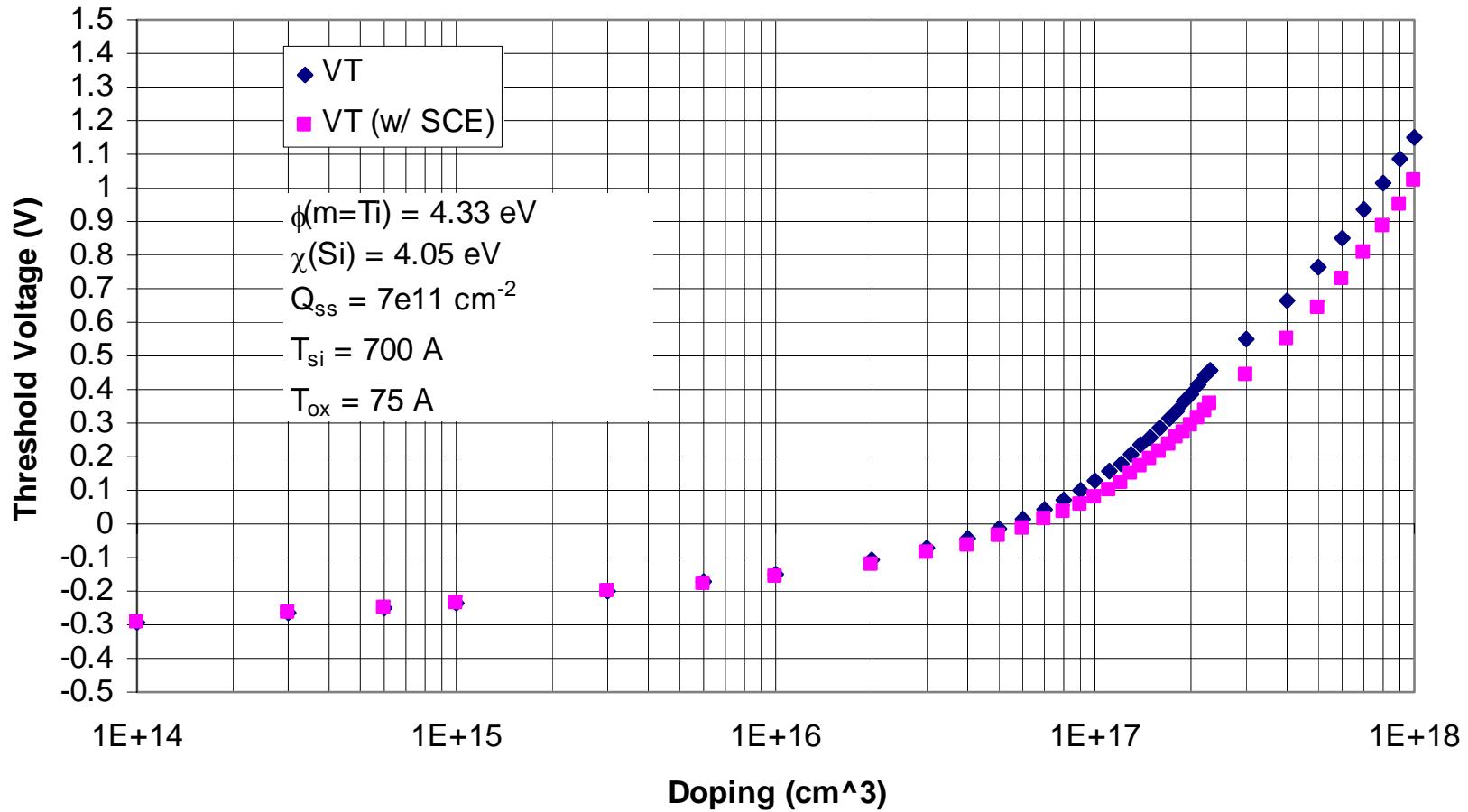
Activation of source/drain impurities via excimer laser annealing is necessary because the high temperatures used in conventional thermal annealing will melt the Al gate. The main disadvantage of laser annealing is the low throughput of wafers, which is an important consideration for manufacturability.

$\lambda = 308 \text{ nm XeCl Excimer Laser}$



Threshold Voltage Calculation

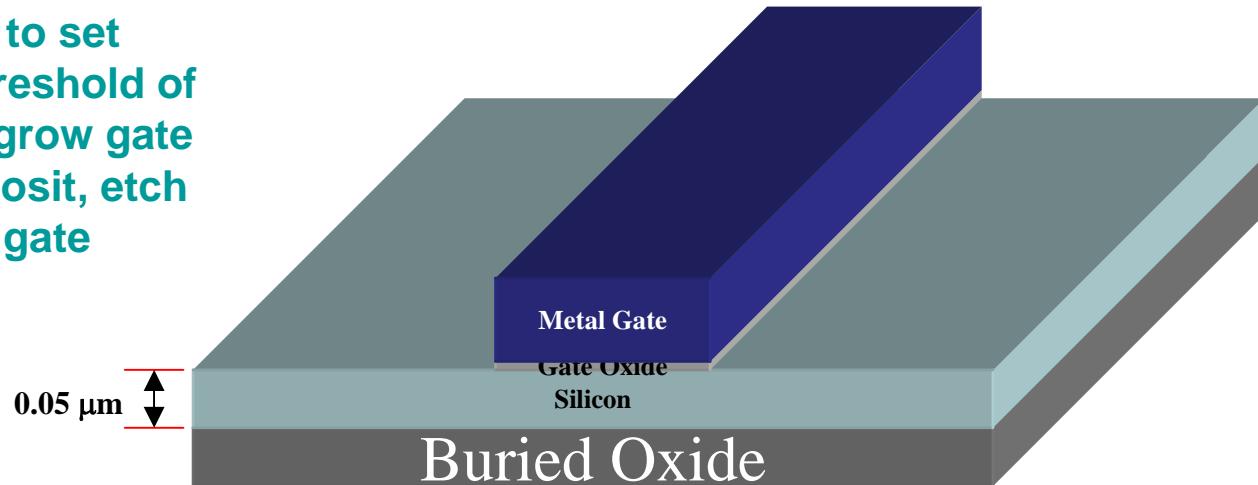
Threshold Voltage Calculations for nMOS with Short Channel Effects



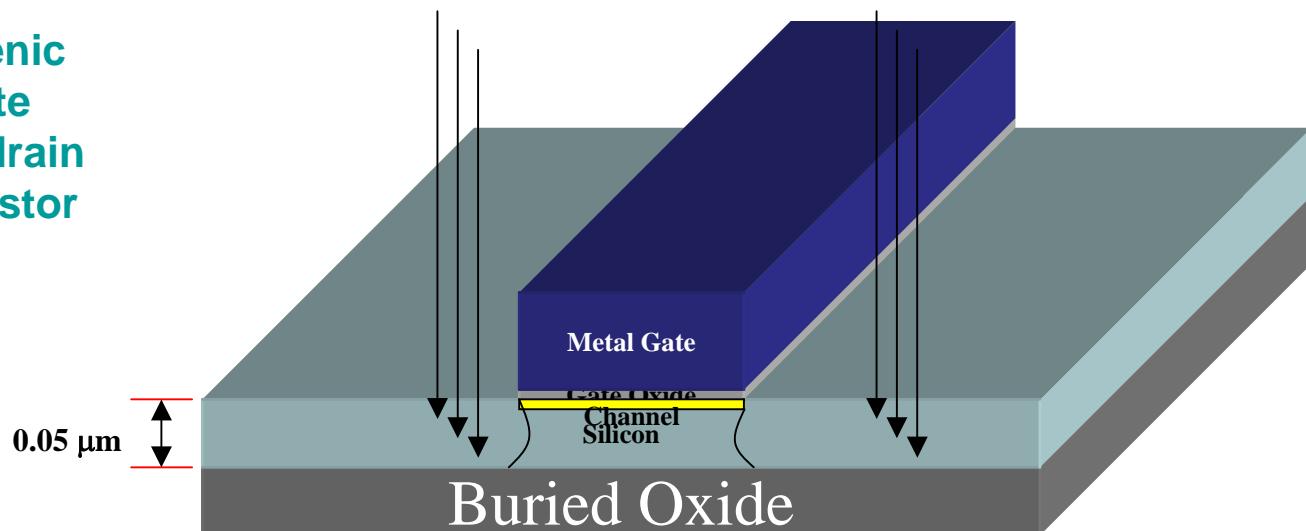
$$VT = \Phi_{MS} - \frac{Q_{ss}}{C_{ox}} + 2\Phi_f + \frac{qN_a x_{dmax}}{C_{ox}}$$

MOSFET Fabrication Process

Implant Si to set
voltage threshold of
MOSFET, grow gate
oxide, deposit, etch
aluminum gate

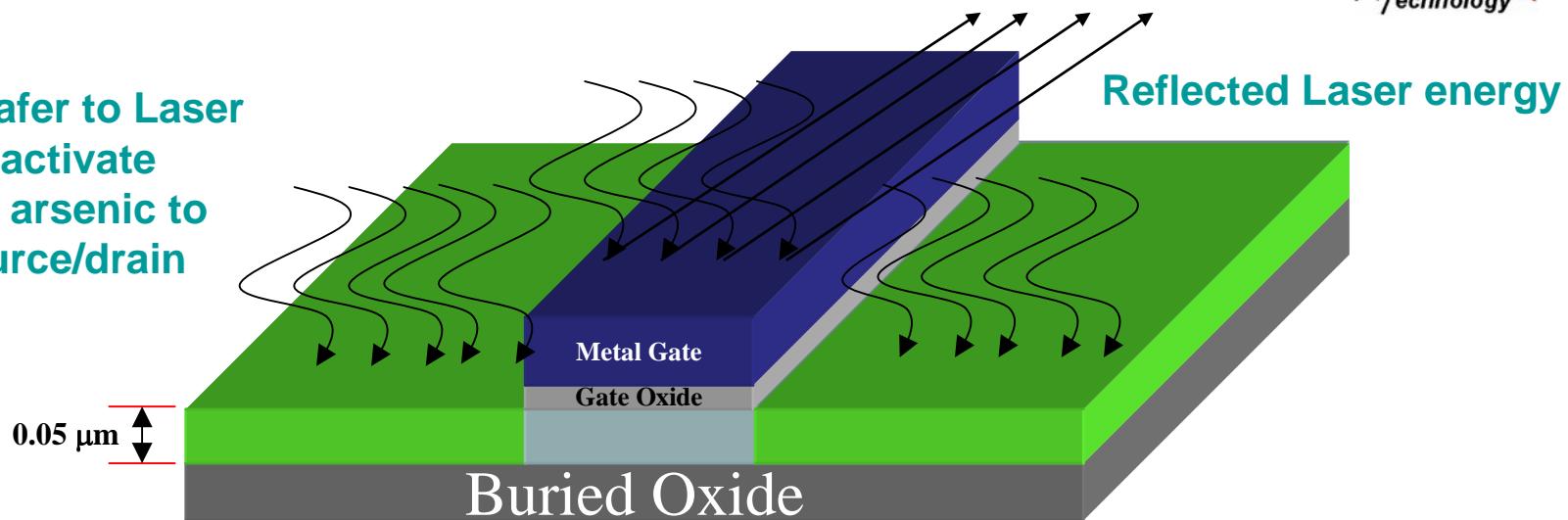


Implant arsenic
ions to create
the source/drain
of the transistor

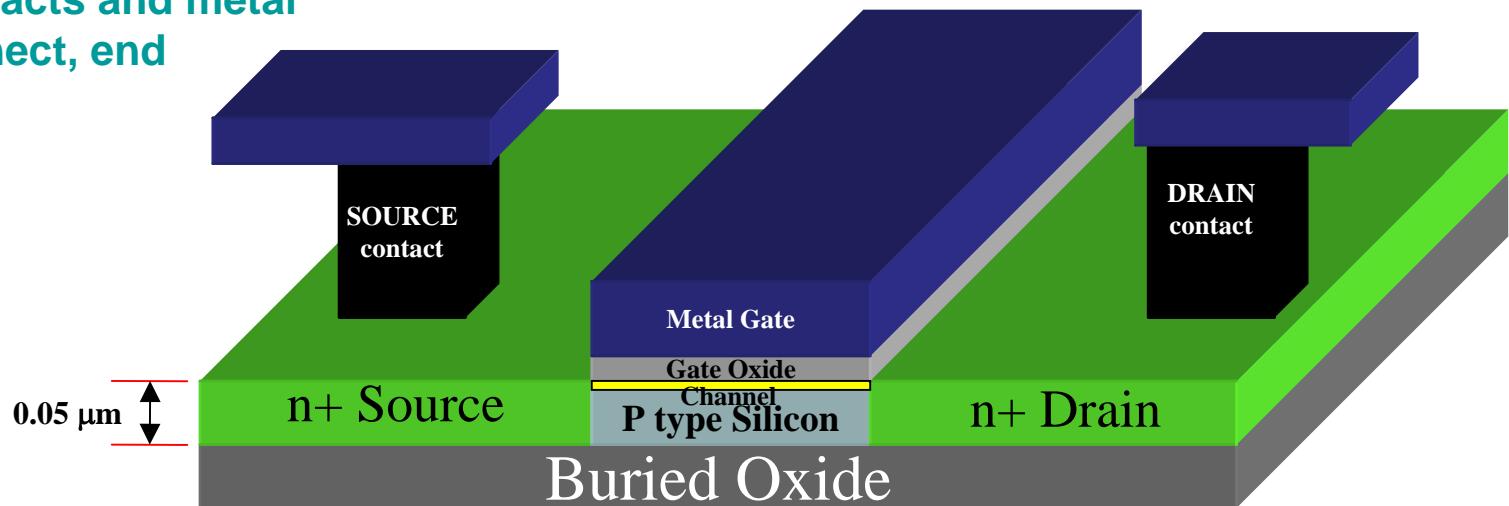


Laser Annealing Process

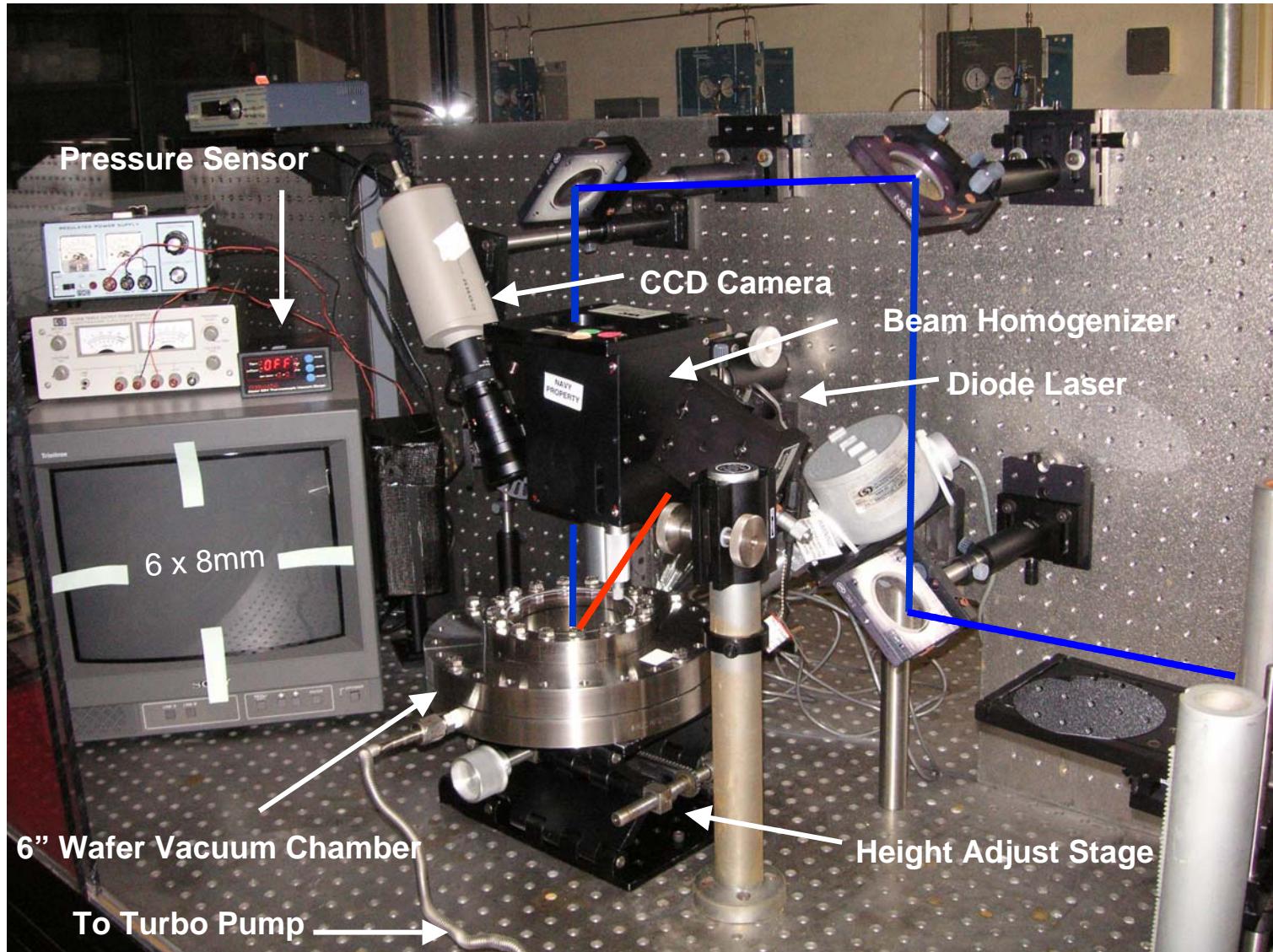
Expose wafer to Laser energy to activate implanted arsenic to define source/drain regions.



Deposit oxide, pattern, etch contacts and metal interconnect, end product.

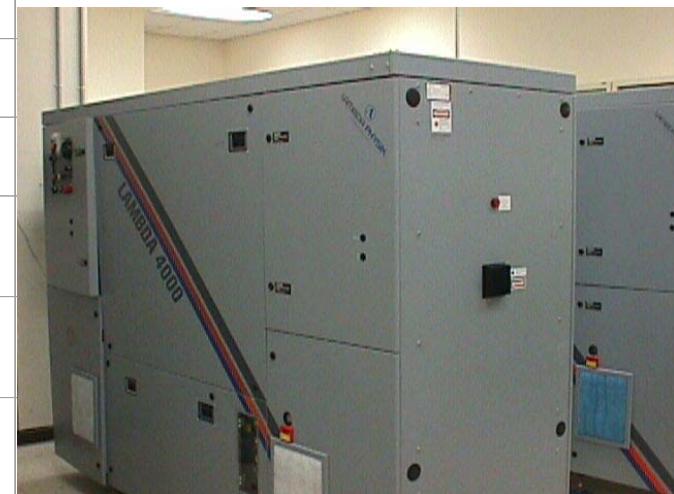


Laser Annealing System

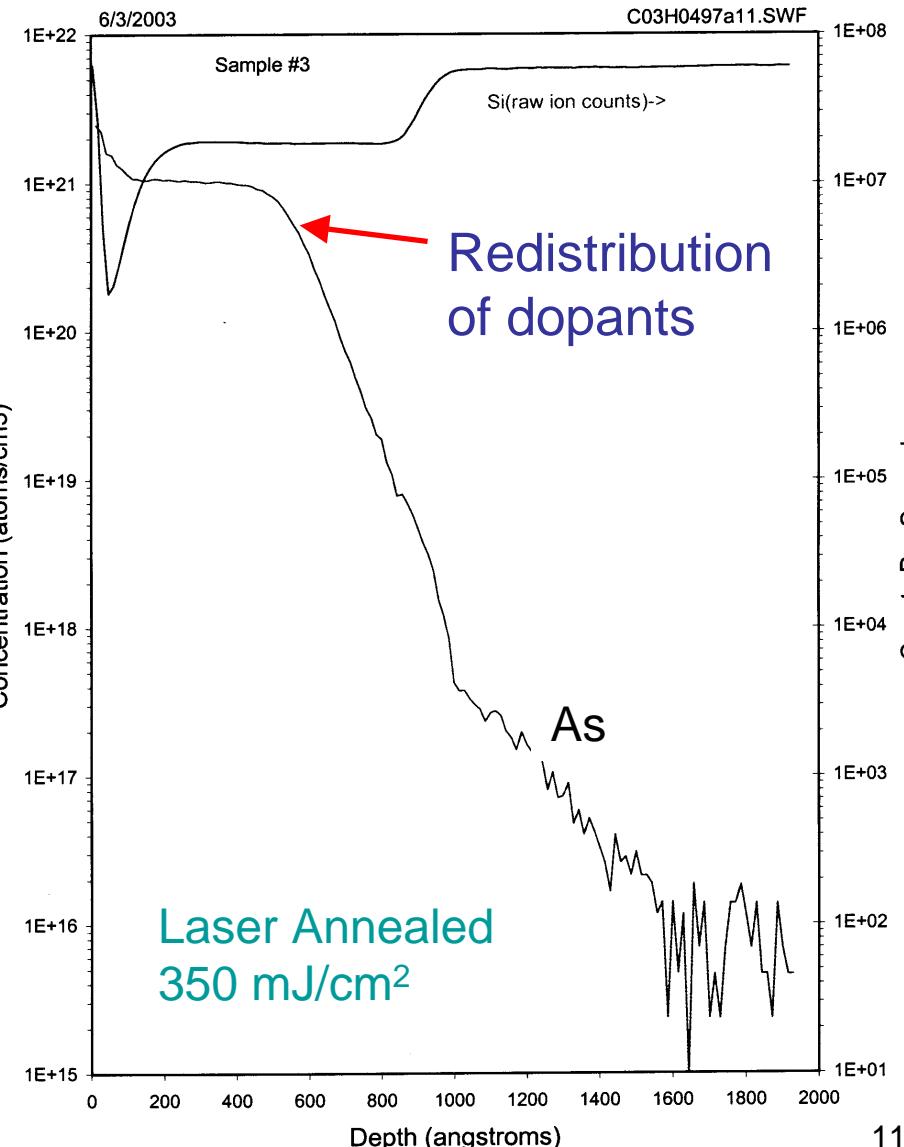
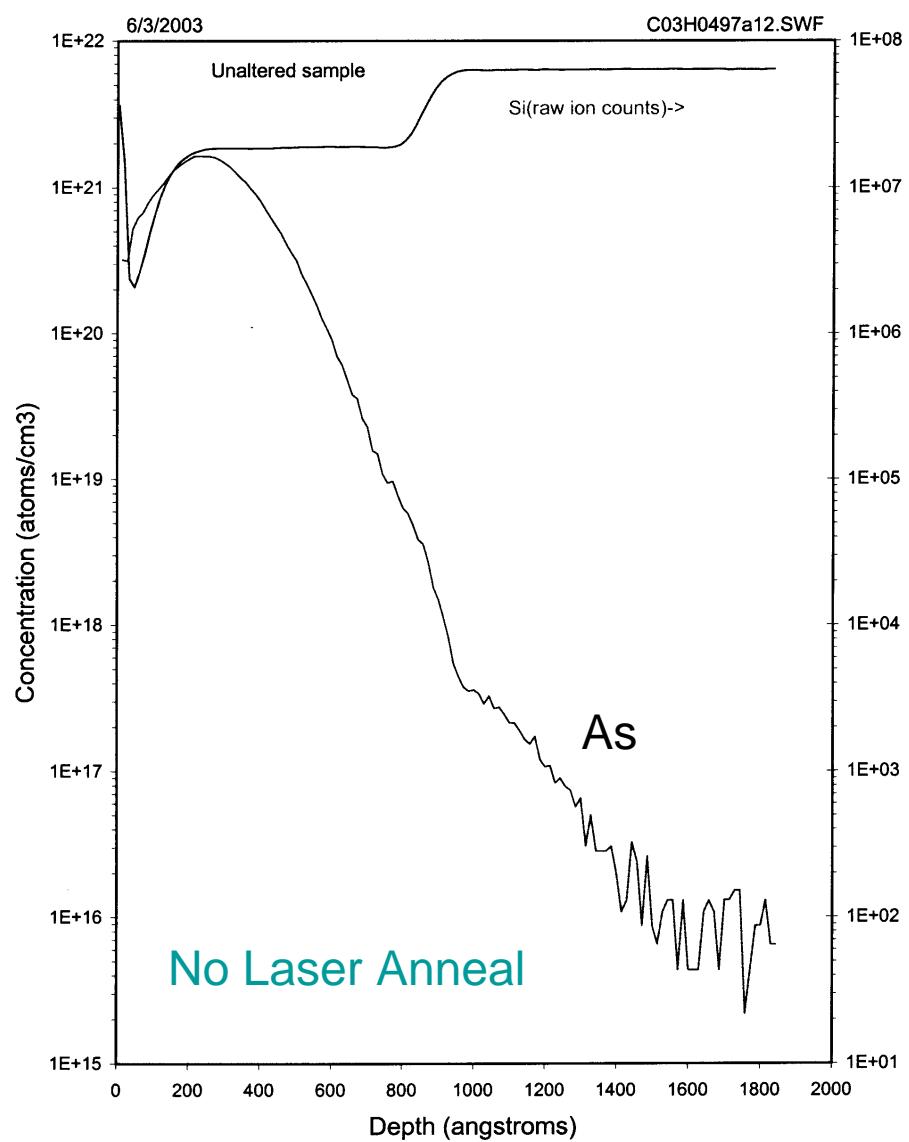


Laser Parameters

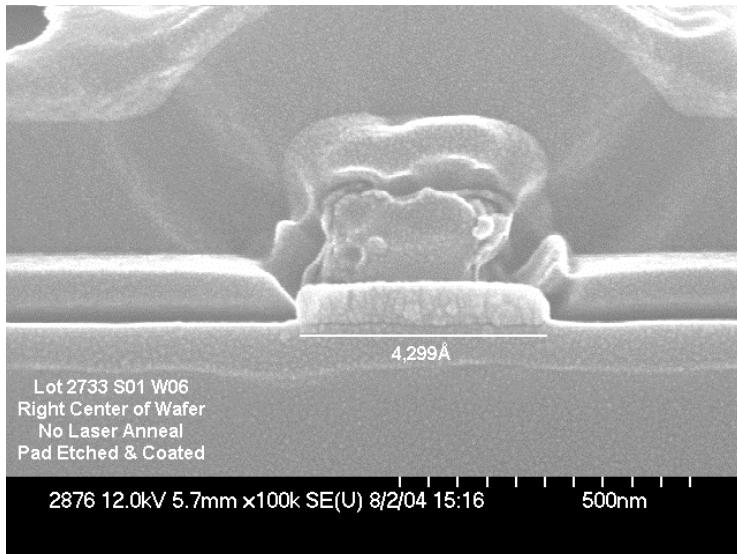
SOI Wafers Characteristics	
Material	6-in SOI Wafer
Orientation	<001>
Si Thickness	700 Å
SiO ₂ Thickness	on a 3800Å-layer of SiO ₂
Laser	Excimer, 308 nm XeCl
Pulse Energies	Up to 450 mJ
Fluence	Ranged from 300 to 400 mJ/cm ²
Pulse Rep. Rate	1 Hz, ~20 ns pulse length
Pressure	200 mtorr (processing chamber)



SIMS Analysis



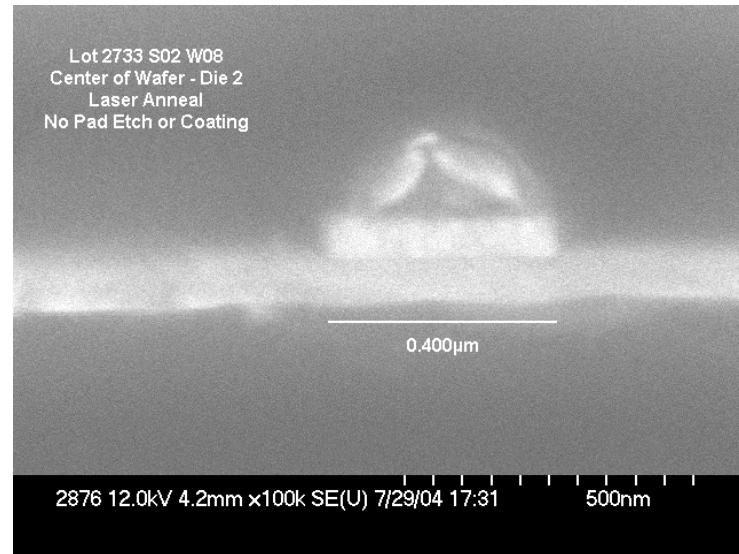
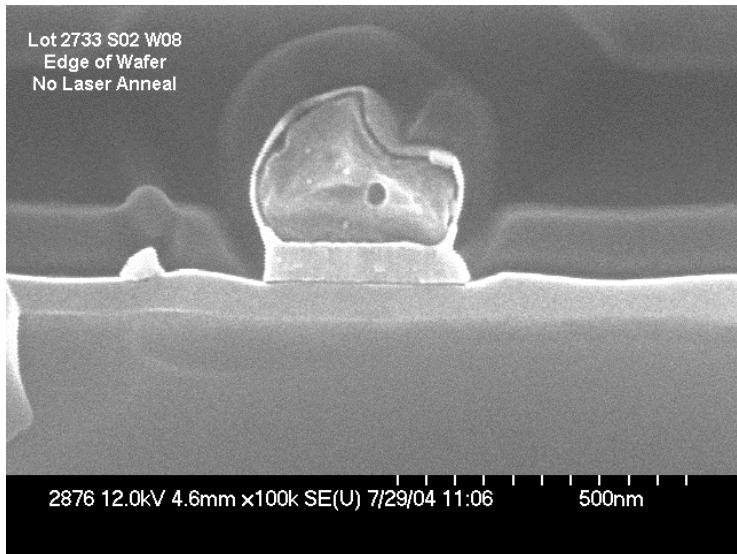
SEM Images



0.25-micron drawn gate length.

0.40-micron actual gate length.

Lithography and PVD Gate metal etch process needs optimization.



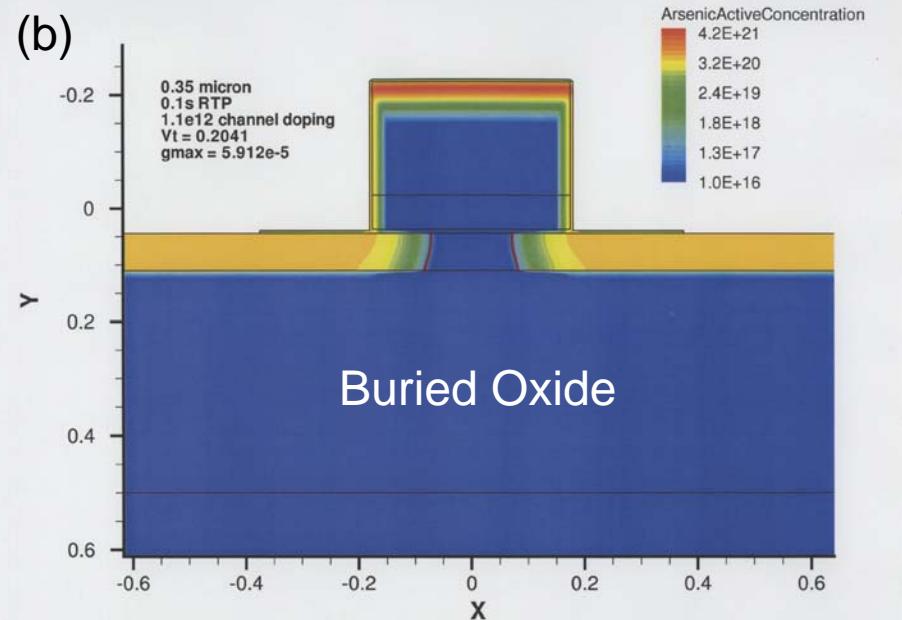
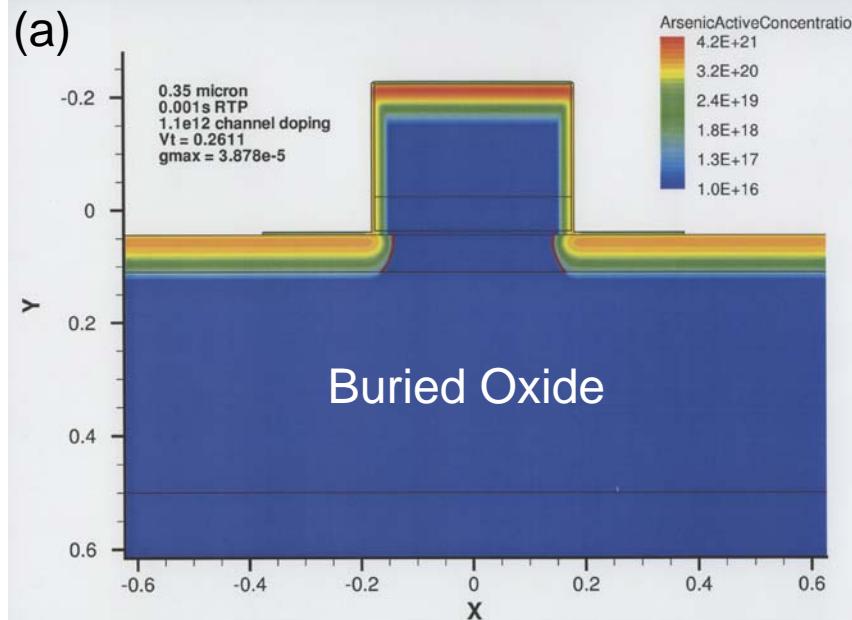
Summary of Device Transfer Characteristics

Energy	Pulses	W (μm)	L(μm)	Vt (V)	SS (mV/dB)	Ion/Ioff	Comments
350	3	10	10	X	X	10^6	Shorted
		3	10	0.24	79.1		
		3	0.8	X	X		
		10	0.25	0.19	101.7		
		5	0.25	0.18	91.9		
		3	0.25	0.13	92.7		
350	5	10	10	0.24	85.2	10^6	Shorted Shorted
		3	10	0.23	80.1		
		3	0.8	0.17	X		
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.11			
375	3	10	10	0.21		10^6	Shorted Shorted
		3	10	0.19			
		3	0.8	0.19			
		10	0.25	X	X		
		5	0.25	X	X		
		3	0.25	0.16			
375	5	10	10	0.22	78.4	$10^{6.5}$	
		3	10	0.22	79.4		
		3	0.8	0.19	73.4		
		10	0.25	X	X		
		5	0.25	0.19	95.2		
		3	0.25	0.18	97.7		

Summary of Device Transfer Characteristics

Energy	Pulses	W (μm)	L(μm)	Vt (V)	SS (mV/dB)	Ion/Ioff	Comments
400	3	10	10	0.20	79.9	$10^{6.5}$	
		3	10	0.20	78.4	10^6	
		3	0.8	0.18	71.7	10^7	
		10	0.25	X	X		Shorted
		5	0.25	X	X		Shorted
		3	0.25	0.16	111.1	10^6	
400	5	10	10	0.18	81	10^6	
		3	10	0.19	77.9	10^6	
		3	0.8	0.20	87.2	$10^{6.5}$	
		10	0.25	X	X		Shorted
		5	0.25	X	X		Shorted
		3	0.25	0.07	105.3	$10^{6.5}$	
450	3	10	10	0.18	77.6	10^7	
		3	10	0.19	76.5	10^6	
		3	0.8	0.25	74.4	10^7	
		10	0.25	X	X		Shorted
		5	0.25	X	X		Shorted
		3	0.25	0.19	104.5	10^7	
450	5	10	10	0.21	77.4	10^7	
		3	10	0.20	77.6	10^6	
		3	0.8	0.18	70.7	10^7	
		10	0.25	X	X		Shorted
		5	0.25	X	X		Shorted
		3	0.25	0.16	103	10^6	

Process Simulations

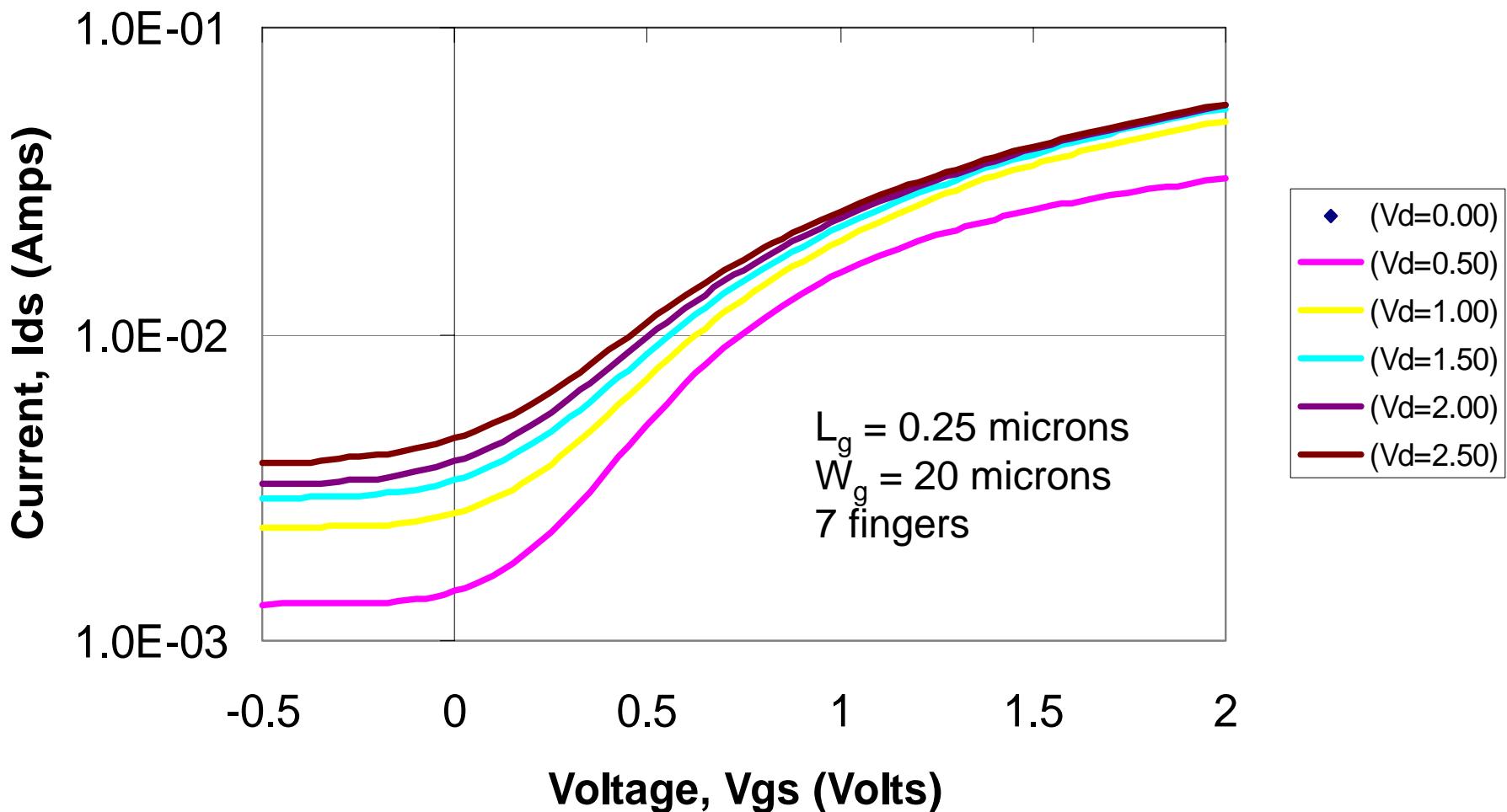


Previous studies found in the literature show junction temperatures reaching 1200 °C
 Kim et al., *IEEE Trans. Elec. Dev.*, 1748, 49 (2002).

Rapid Thermal Processing (RTP) simulation using integrated systems engineering (ISE) DIOS (a multidimensional process simulator for semiconductor devices) shows noticeable As dopant diffusion under the gate for a 0.1-sec RTP, which can explain shorting of submicron devices. However, laser pulse length are several magnitudes smaller (20 to 30 ns) where the source/drain profile is better represented by Figure (a).

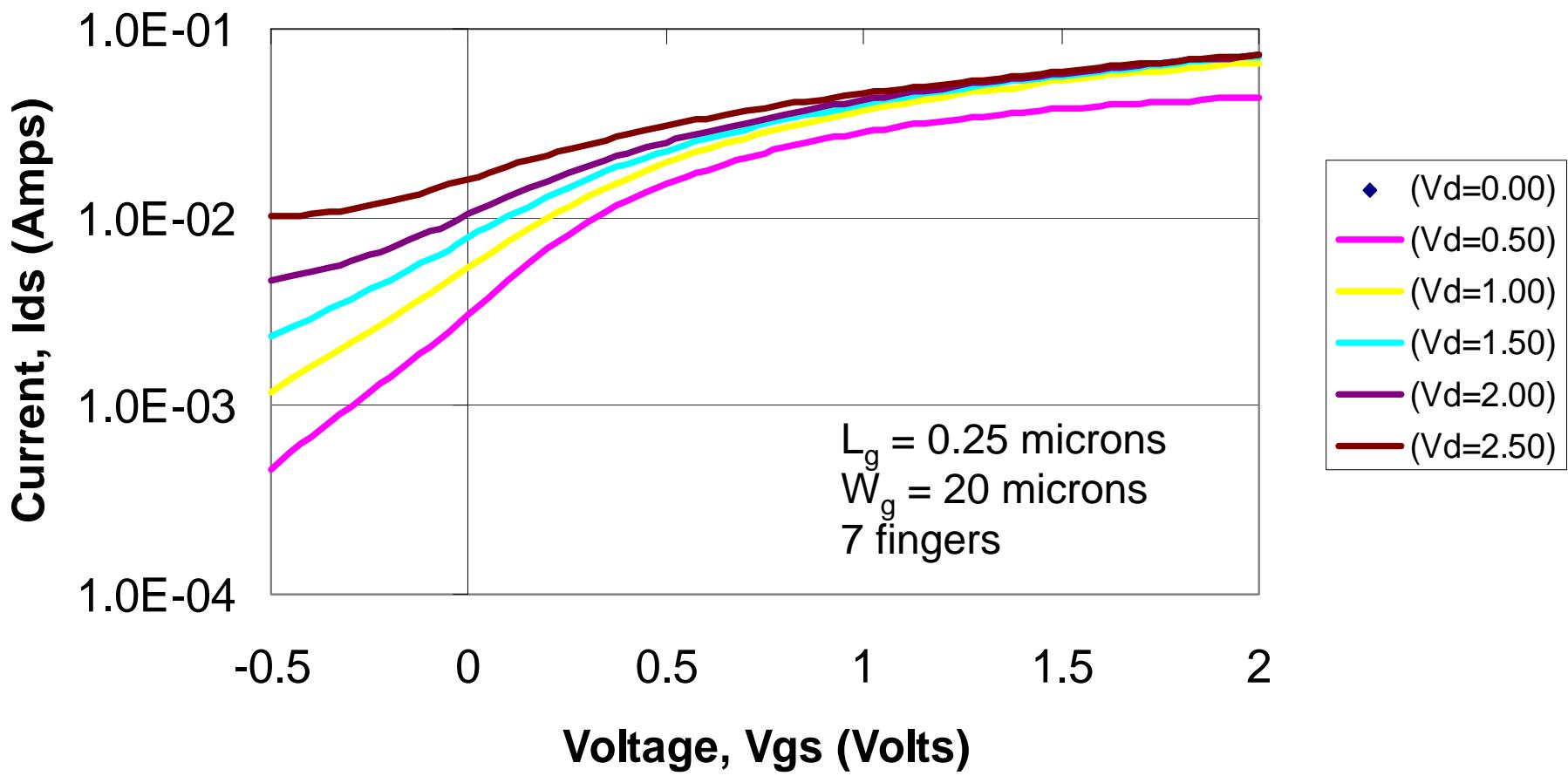
Metal-Gate Device Transfer Characteristics

V_{gs} vs I_{ds}



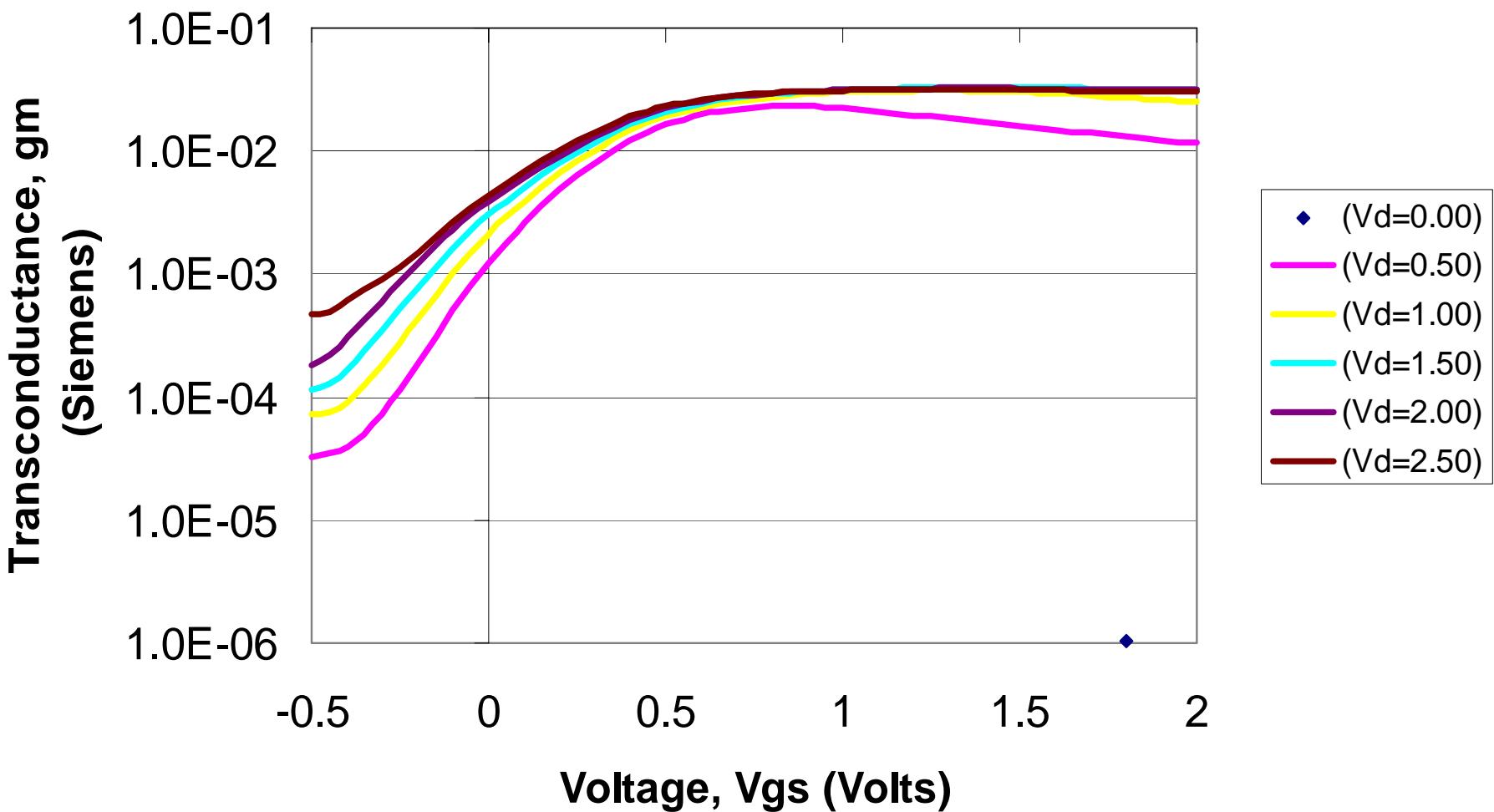
Polygate Device Transfer Characteristics

V_{gs} vs I_{ds}



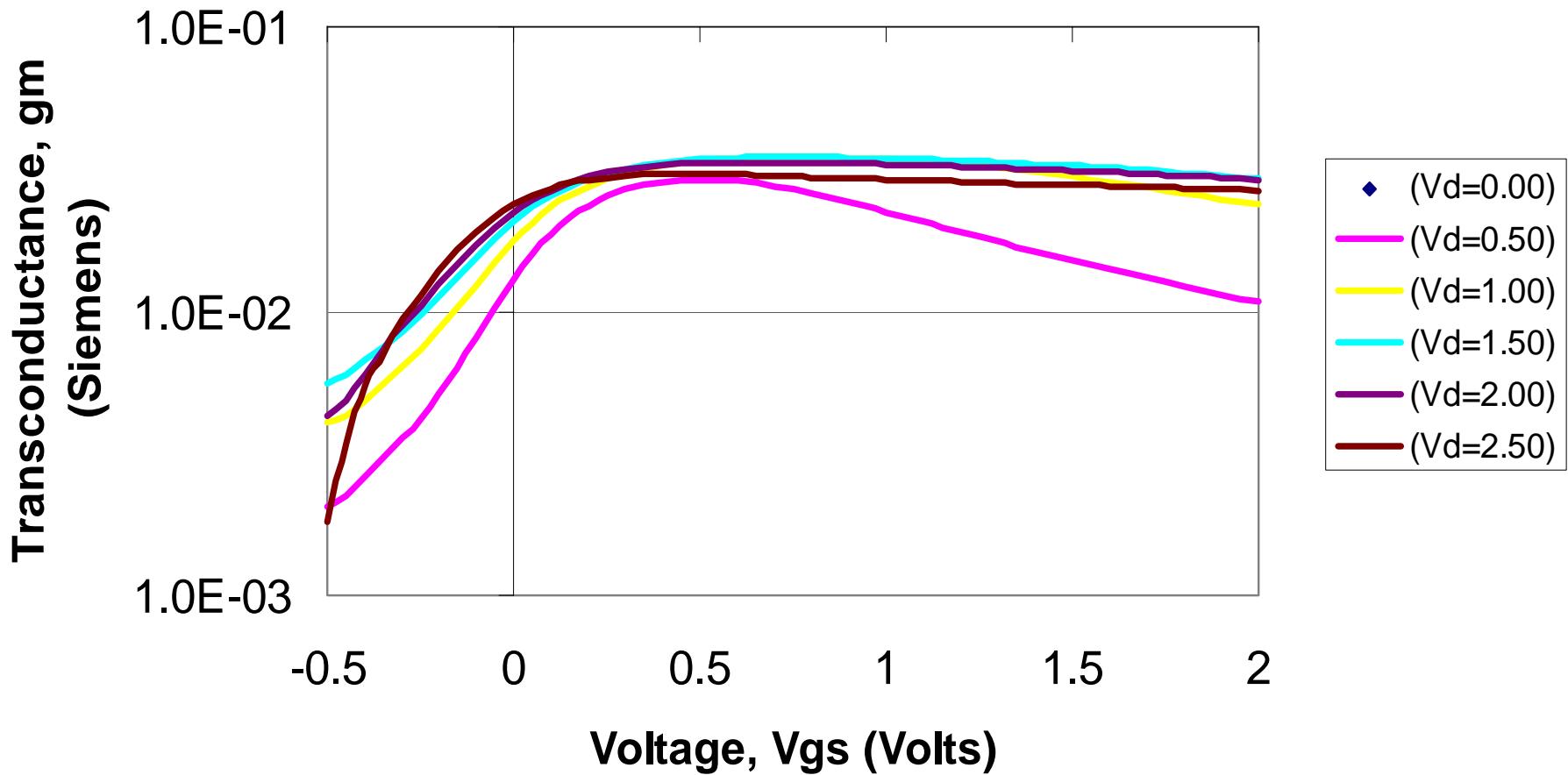
Metal-Gate Device Transconductance

V_{gs} vs g_m



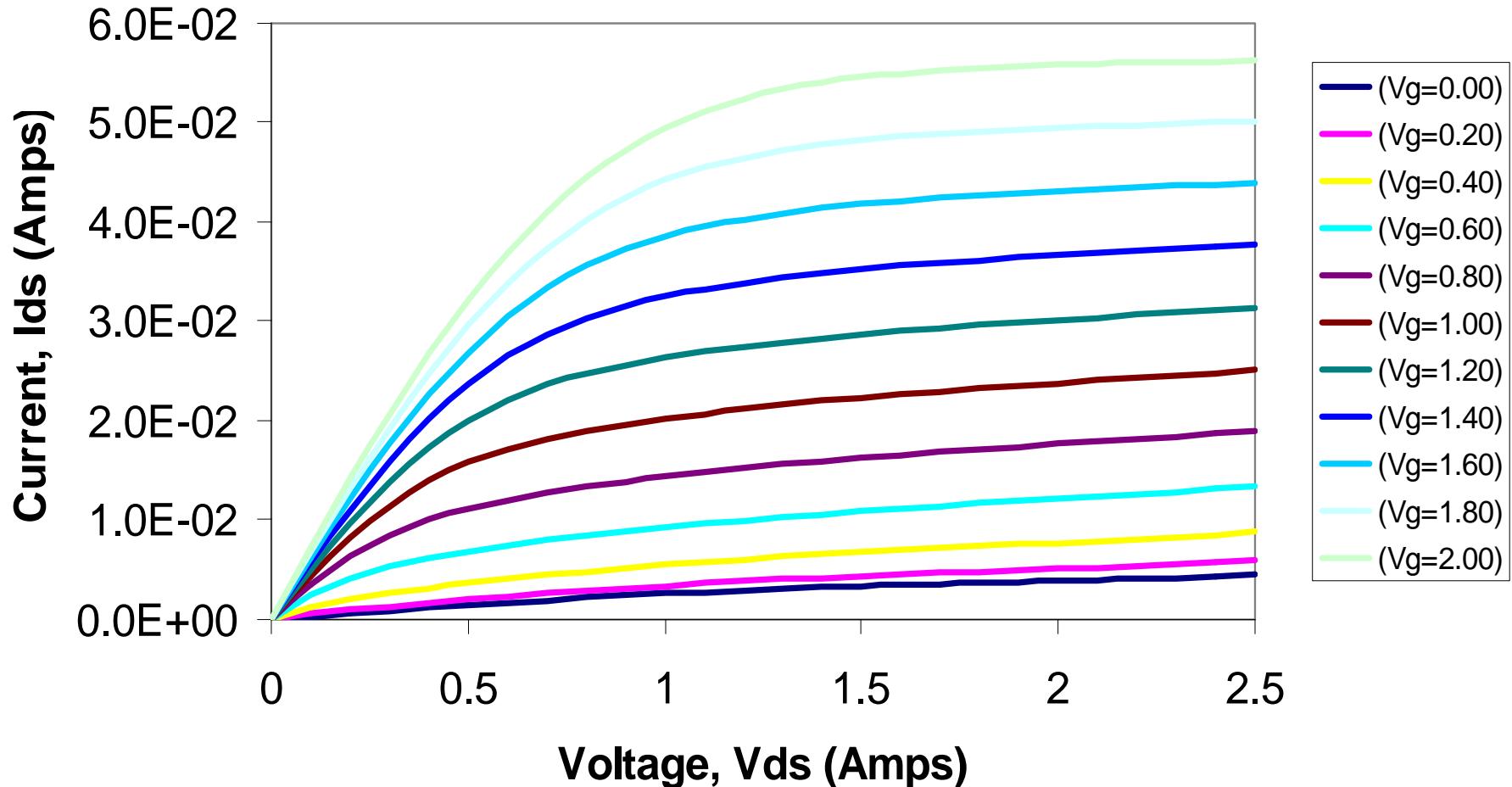
Polygate Device Transconductance

V_{gs} vs gm



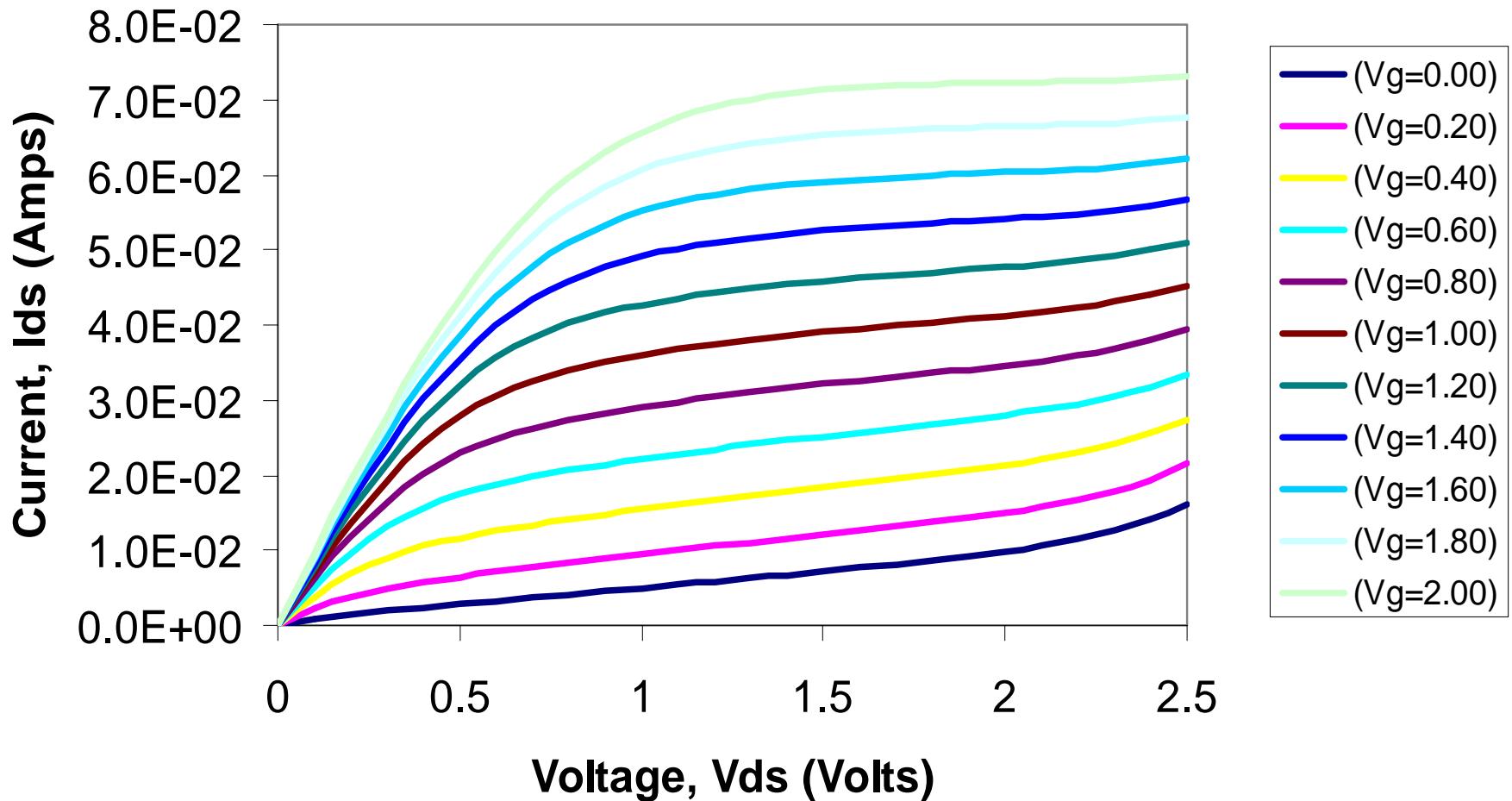
Metal-Gate Device Output Characteristics

V_{ds} vs I_{ds}



Polygate Device Output Characteristics

Vds vs Ids



RF Figures of Merit

Unity Current Gain Frequency

$$f_t = \frac{g_m}{2\pi (C_{gs} + C_{gd} + C_{gb})}$$

Speed

Decrease C'_s  Increase f_t

Unity Power Gain Frequency

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + g_{ds} [R_g + R_s]}}$$

RF Gain

Decrease R_g  Increase f_{max}

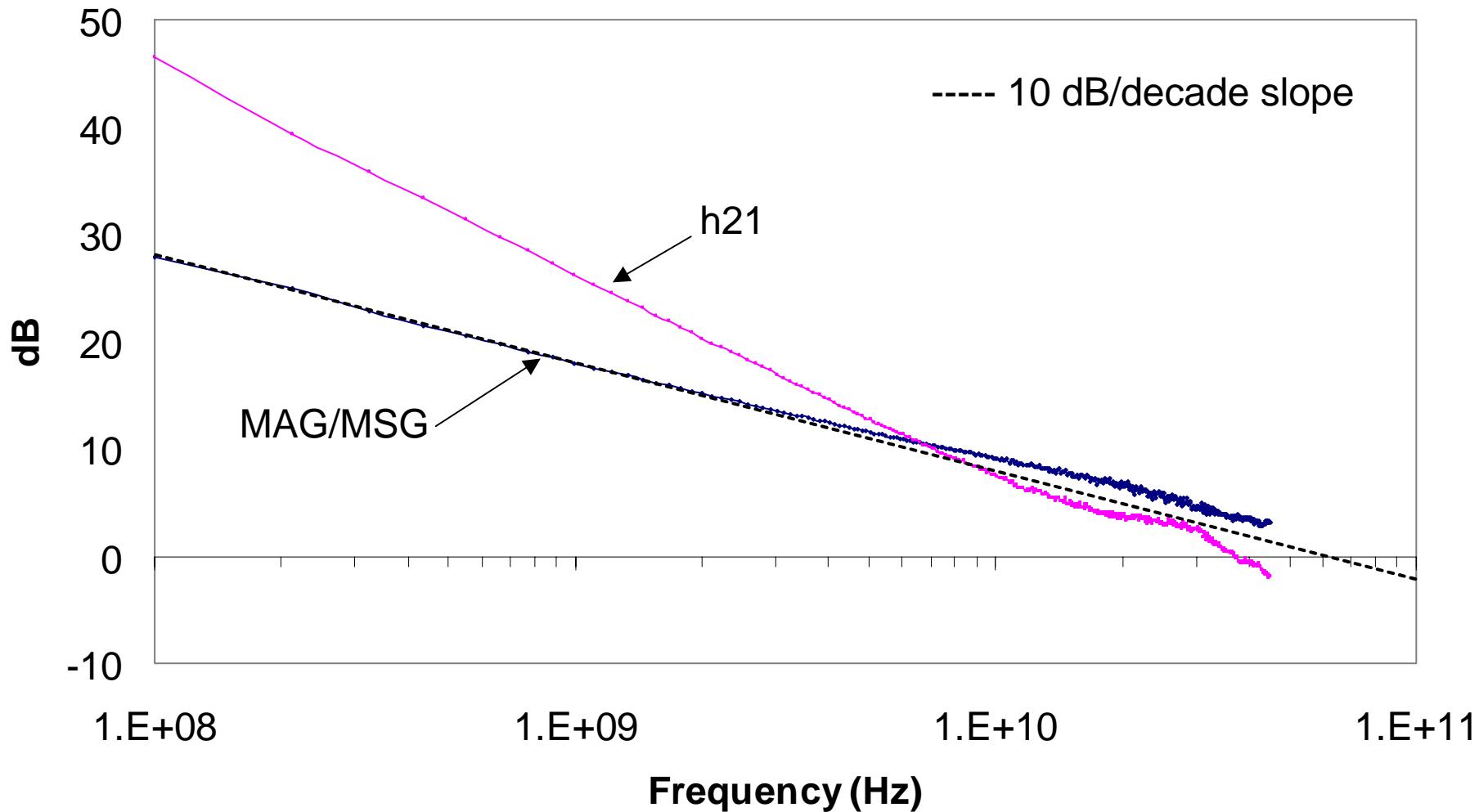
Minimum Noise

$$F_{min} = 1 + k \frac{f}{f_t} \sqrt{g_m [R_s + R_g]}$$

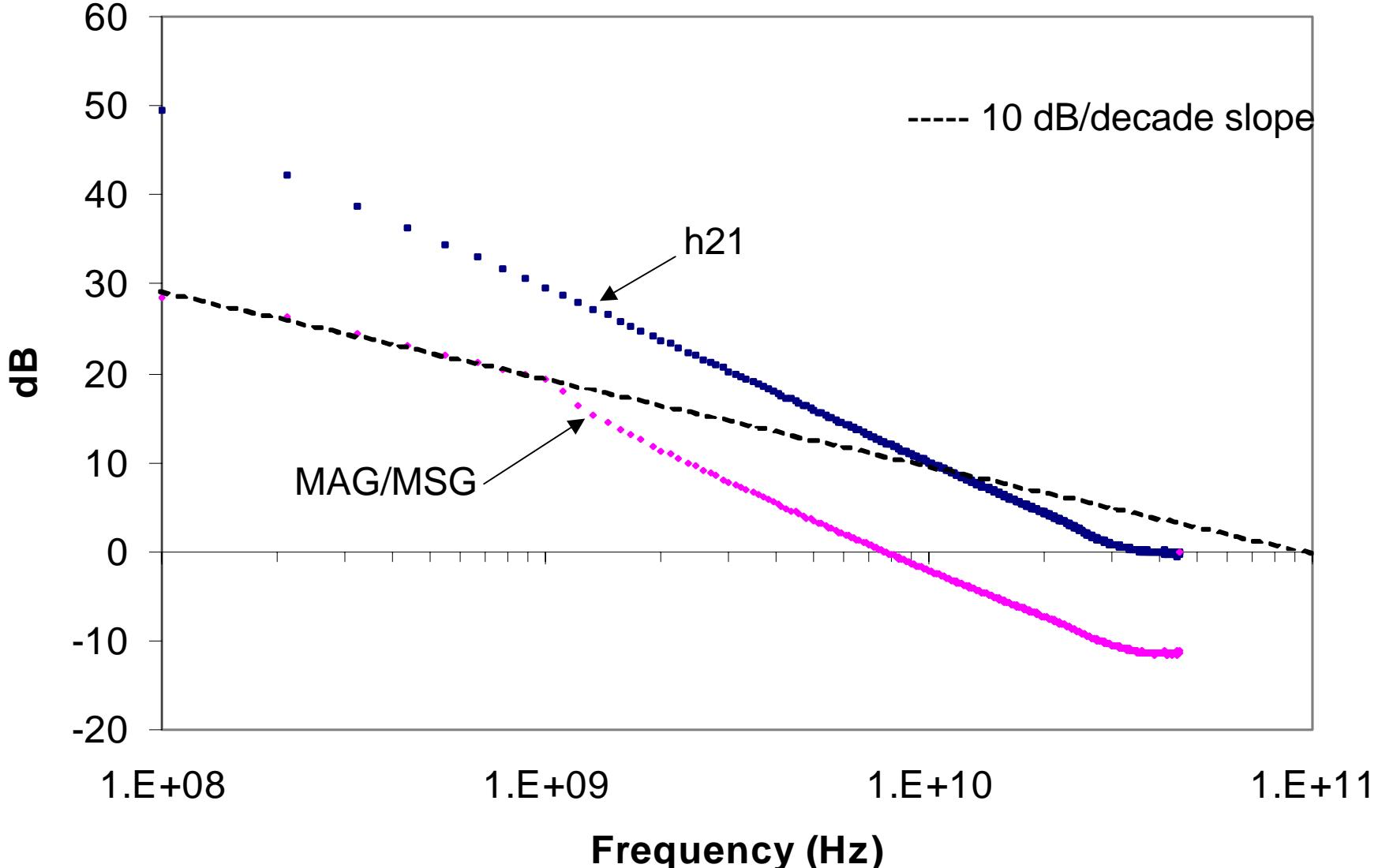
Microwave Noise

Decrease R_g  Decrease F_{min}

RF Characterization of Metal-Gate Device



RF Characterization of Polysilicon Gate Device



Conclusions

1. Performed DC and RF characterization of laser annealed MOS SOI devices with Ti/TiN/Al gate.
2. DC device characteristics were found to be relatively independent of laser fluence.
3. Device shorting occurs for 0.25-micron drawn gate length devices.
4. ISE DIOS Process simulation indicates laser-induced Source/Drain shorting is not possible for 0.25-micron devices due to nanosecond laser pulses. Further studies need to be conducted to explain the low yield of submicron devices.
5. nMOS devices exhibit I_d values of over 50 mA, F_t values of over 25 GHz, and F_{max} values of 60 GHz.

REPORT DOCUMENTATION PAGE

*Form Approved
OMB No. 0704-01-0188*

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden to Department of Defense, Washington Headquarters Services Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE (DD-MM-YYYY) 04-2005	2. REPORT TYPE Final	3. DATES COVERED (From - To)
---	--------------------------------	-------------------------------------

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
------------------------------	----------------------------

DC AND RF CHARACTERIZATION OF LASER ANNEALED METAL-GATE
SOI CMOS FIELD-EFFECT TRANSISTORS

6. AUTHORS	5d. PROJECT NUMBER
-------------------	---------------------------

R. P. Lu J. F. Rowland
B. W. Offord S. D. Russell
J. D. Popp
A. D. Ramirez

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
---	---

SSC San Diego
San Diego, CA 92152-5001

TD 3196

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
--	---

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5660

ONR

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

This is a work of the United States Government and therefore is not copyrighted. This work may be copied and disseminated without restriction. Many SSC San Diego public release documents are available in electronic format at <http://www.spawar.navy.mil/sti/publications/pubs/index.html>

14. ABSTRACT

The conventional polysilicon gate in a MOSFET has been replaced by an aluminum metal gate which offers higher RF performance through the reduction of gate resistance. Pulsed excimer laser annealing of the source and drain was then used to avoid conventional furnace annealing that would melt the aluminum metal gate. CMOS field-effect transistors utilizing metal-gates were fabricated in SOI technology down to 0.25-micron gate lengths. The DC characteristics of devices with 10-micron gate lengths were consistently well-behaved. The 0.25-micron devices were found to be more sensitive to the laser energy which showed up in the DC measurements in threshold voltage variations and larger leakage currents in the subthreshold characteristics. At higher laser fluences, Technology Computer-Aided Design (TCAD) simulations show excessive lateral diffusion, explaining the observed effects. RF results of the drawn 0.25-micron metal-gate devices have an F_t and F_{max} of 25 GHz and 60 GHz, respectively. Similar devices with polysilicon gates were fabricated and characterized for comparison. RF results of the drawn 0.25-micron polysilicon-gate devices have an F_t and F_{max} of 34 GHz and 7 GHz, respectively. This device processing advance offers a deeply scalable technology for future "system-on-a-chip" applications.

15. SUBJECT TERMS

Mission Area: Microelectronics

short channel effects silicon-on-insulator metal gates implanted dopants
parasitic resistance parasitic capacitance laser annealing nMOS device

16. SECURITY CLASSIFICATION OF:	17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
--	-----------------------------------	----------------------------	--

a. REPORT U	b. ABSTRACT U	c. THIS PAGE U	19a. NAME OF RESPONSIBLE PERSON A. D. Ramirez
-----------------------	-------------------------	--------------------------	---

19B. TELEPHONE NUMBER (Include area code) (619) 553-7561
--

INITIAL DISTRIBUTION

20012	Patent Counsel	(1)
21511	J. Andrews	(1)
21512	Library	(2)
21513	Archive/Stock	(3)
285	S. D. Russell	(5)
2853	A. D. Ramirez	(5)
2876	B. W. Offord	(5)
2876	J. D. Popp	(5)
2876	J. F. Rowland	(5)

Defense Technical Information Center
Fort Belvoir, VA 22060-6218 (4)

SSC San Diego Liaison Office
C/O PEO-SCS
Arlington, VA 22202-4804 (1)

Center for Naval Analyses
Alexandria, VA 22311-1850 (1)

Office of Naval Research
ATTN: NARDIC
Philadelphia, PA 19111-5078 (1)

Government-Industry Data Exchange
Program Operations Center
Corona, CA 91718-8000 (1)

Approved for public release; distribution is unlimited.